This Application has been carefully reviewed in light of the Office Action mailed February 21, 2002. Claims 1-30 were pending and stand rejected. Reconsideration and allowance of all pending claims is respectfully requested in view of the following remarks.

REMARKS

Claims 1-4, 7-11, 13-20 and 22-30 were rejected under 35 U.S.C. 102 as being anticipated by *Gardner* et al, U.S. Patent 5,350,484. Claims 5, 12 and 21 under 35 U.S.C. 103(a) were rejected as being unpatentable over *Gardner* et al. Claim 6 was rejected under 35 U.S.C. 103(a) as being unpatentable over *Gardner* in view of *Ye*, et al, U.S. Patent 6,010,603. Applicants respectfully traverse these rejections.

The cited reference does not teach each and every limitation of Claim 1, as amended, and for this reason Claim 1 is allowable. Claim 1 recites "wherein exposing the semiconductor device to a treatment process comprises: exposing the semiconductor device to a substantially inert atmosphere; and heating the semiconductor device to between 300 and 800 degrees Celsius to remove the compound." These limitations are not shown by the cited references. The Office Action concedes these limitations are not shown by *Gardner* ("*Gardner* fails to teach wherein exposing the semiconductor-device to a treatment process comprising: exposing the semiconductor device to a substantially inert atmosphere; and heating the semiconductor device to between 300 and 800 degrees Celsius to remove the compounds.") Office Action at Page 4, Paragraph 16. Nor does *Ye*, which was used in the Office Action to reject former Claim 6, teach this missing limitation. The cited portion of *Ye* involves the "use of a reactive ion etch component in patterned copper etching" in which gases fed to the etch chamber include a not insubstantiated amount of chlorine, which is not inert. Because the purpose of feeding these gases to the etch chamber is to perform a reactive etch and this gas is not inert, *Ye* does not show exposing the semiconductor device to a substantially inert atmosphere. For this reason, the rejection is improper.

The Office Action asserts that "*Ye* teaches exposing the semiconductor device to a substantially inert atmosphere" and "it would have been obvious to one of ordinary skill in the art to incorporate the compound removal process of *Ye* into the *Gardner* semiconductor process because it helps volatize some species of CuClx enabling these species to leave the film surface," but neither of these statements are correct. First, as demonstrated above, *Ye*

does not teach exposing the semiconductor device to a substantially inert atmosphere because the reactive etch process asserted to constitute exposure to an inert atmosphere involves not insubstantial amounts of a non-inert gas and because the purpose of the reactive etch process involves causing a chemical reaction in the etch chamber – that is why the process is referred to as a "reactive" etch process. Second, it would not have been obvious to modify *Gardner* in view of *Ye* to provide the claimed two-step process of (1) forming a compound and (2) removing the compound by exposing the device to a substantially inert atmosphere and heating the device to the claimed temperature range while exposed to the substantially inert atmosphere. This is so because *Ye* involves removing the compound at the same time as it is being formed – this is what is referred to as a reactive etch process. In addition, as described above, *Ye* fails to teach the missing limitation of exposing the device to a substantially inert atmosphere and therefore the combination would not have been motivated.

For at least the above reasons, Claim 1 and the claims depending therefrom, Claims 2-5 and 7-10 are allowable. Reconsideration and favorable action are requested.

Claim 11 recites "wherein exposing the electronic device to a treatment process comprises: exposing the electronic device to a substantially inert atmosphere; and heating the semiconductor device between 300 and 800 degrees Celsius while the semiconductor device is exposed to the substantially inert atmosphere," which as described above is not taught by the cited reference. Therefore, Claim 11 and the claims depending therefrom, Claims 12-17, are allowable. Reconsideration and favorable action are requested.

Claim 18, as amended, is allowable because the cited references do not teach and every limitation of that claim. Claim 18, as amended, recites "exposing the electronic device to a plasma and at least one other gas selected from the group of inert gases and nitrogen, the plasma converting an unmasked portion of the conductive layer into a compound and the at least one other gas enhancing the conversion into the compound." *Gardner* does not teach this limitation. *Gardner* does not disclose the addition of an inert gas or nitrogen to the plasma to enhance the compound-forming process, nor would such an addition to *Gardner* make sense. *Gardner* involves either ion implantation or a reactive ion etch. Ion implantation does not involve plasma. Reaction ion etching does involve high energy plasma; however, the addition of nitrogen or inert gases to high energy plasma does not enhance the formation of the compound, as claimed, and therefore one would not be

motivated to add such a gas to the process in *Gardner*. However, the invention recognizes that low energy plasma, which relies principally on a chemical reaction to form a compound to be removed, rather than the insertion of ions, as is the case in *Gardner*, benefits from the addition of nitrogen or inert gas.

Ye clearly does not show the two step process of forming a compound and then subsequently removing it, but rather involves splitting the copper layer by layer, and one would not be motivated by *Ye* to add nitrogen or an inert gas to the process of *Gardner* because, as described above, formation of a compound for later removal by a high energy reactive ion etch would not benefit from the use of nitrogen or inert gases.

New claim 31 is allowable because none of the cited references teach "exposing, by a plasma deposition reactor, the device to a plasma, the plasma converting the unmasked portions of the conductive layer into a compound." Support for this new claim is found at page 8, lines 21-29. *Gardner* involves either ion implantation or reactive ion etching (see Abstract and Claims). Ion implantation does not include exposing a device to a plasma. Reactive ion etching includes high energy plasma, and in *Gardner*, relies principally on ion bombardment to form the copper compound that will be removed. In contrast, exposing a device to plasma by a plasma deposition reactor involves low energy plasma, which relies principally on a chemical reaction to form the copper compound that will be removed. Because *Gardner* involves only high energy plasma it clearly does not show the use of a plasma deposition reactor, nor would it be obvious to modify *Gardner* to use a plasma deposition reactor. Because *Gardner* focuses on ion bombardment as the mechanism to create the compound, one would not have been motivated to use a plasma deposition reactor with *Gardner*, as such a plasma deposition reactor would not create the high energy plasma required. For at least this reason, Claim 31 is allowable. Favorable action is requested.

New Claim 32 is allowable because none of the cited references show "exposing the device to a low energy plasma." Support for this new claim is provided at page 8, lines 21-29. It is respectfully submitted that one of skill on the art would understand that plasma deposition is one example of utilizing a low energy plasma. As described above, the cited references do not utilize low energy plasma, but rather rely on high energy ion bombardment (reactive ion etching) or ion implantation. For at least this reason, Claim 32 is allowable. Favorable action is requested.

(reactive ion etching) or ion implantation. For at least this reason, Claim 32 is allowable. Favorable action is requested.

CLAIM OBJECTION

Claim 14 was objected to for informalities. Applicants have amended this claim to address the concerns raised in the Office Action. Favorable action is requested.

CONCLUSION

Applicants have now made an earnest attempt to place this case in condition for immediate allowance. For the foregoing reasons and for other apparent reasons, Applicants respectfully request allowance of all pending claims.

With the filing of two additional independent claims, an additional filing fee of \$102.00 is due. Enclosed is a check in the amount of \$102.00 to cover this fee. The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 02-0384 of Baker Botts L.L.P.

If Examiner believes that prosecution of this Application would be advanced by discussing the Application with Applicant's representative, a telephone call to the undersigned is strongly encouraged.

Respectfully submitted,

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MARKED UP VERSION OF CLAIMS:

1. **(Amended)** A method for forming a conductive pattern for a semiconductor device, comprising:

patterning a mask layer outwardly from a conductive layer of the semiconductor device, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing the semiconductor device to a plasma, the plasma converting the unmasked portions of the conductive layer into a compound; **[and]**

exposing the semiconductor device to a treatment process, the treatment process selectively removing the compound**[.]** **; and**

wherein exposing the semiconductor device to a treatment process comprises:

exposing the semiconductor device to a substantially inert atmosphere; and

heating the semiconductor device to between 300 and 800 degrees Celsius while the semiconductor device is exposed to the substantially inert atmosphere to remove the compound.

2. The method of Claim 1, wherein the conductive layer comprises a copper material.

3. The method of Claim 1, further comprising removing the mask layer from the semiconductor device.

4. The method of Claim 3, wherein removing the mask layer comprises removing the mask layer after removing the compound.

5. The method of Claim 3, wherein removing the mask layer comprises removing the mask layer before removing the compound.

6. **(Canceled)** The method of Claim 1, wherein exposing the semiconductor device to a treatment process comprises:

exposing the semiconductor device to a substantially inert atmosphere; and

heating the semiconductor device to between 300 and 800 degrees Celsius to remove the compound.

7. The method of Claim 1, further comprising providing a barrier layer between the conductive material and a substrate of the semiconductor device.

8. The method of Claim 1, wherein the conductive material comprises a copper material, and wherein exposing the semiconductor device to a plasma comprises exposing the semiconductor device to a chlorine-containing gas.

9. The method of Claim 8, wherein the compound comprises a copper chloride material, and wherein exposing the semiconductor device to a treatment process comprises exposing the semiconductor device to a hydrogen chloride solution to remove the copper chloride material.

10. The method of Claim 1, wherein the mask layer comprises a photoresist material.

11. A method for forming a conductive pattern for an electronic device, comprising:

forming a conductive layer outwardly from a substrate of the electronic device;

patterning a mask layer outwardly from the conductive layer, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing the electronic device to a plasma, the plasma converting the unmasked portions of the conductive layer into a compound;

exposing the electronic device to a treatment process to selectively remove the compound; **[and]**

removing the mask layer from the masked portions of the conductive layer **[.]** **; and**

wherein exposing the [semiconductor] electronic device to a treatment process comprises:

exposing the [semiconductor] electronic device to a substantially inert atmosphere; and

heating the [semiconductor] electronic device to between 300 and 800 degrees Celsius while the [semiconductor] electronic device is exposed to the substantially inert atmosphere to remove the compound.

12. The method of Claim 11, wherein removing the mask layer comprises removing the mask layer before removing the compound.

13. The method of Claim 11, wherein forming a conductive layer comprises forming a copper layer outwardly from the substrate.

14. **(Amended)** The method of Claim 11, wherein **[exposing the electronic device to a plasma comprises exposing the electronic device to a plasma,]** the plasma **[comprising]** **comprises** a gas having an element selected from the halogen group of elements.

15. The method of Claim 11, further comprising providing a barrier layer between the conductive layer and the substrate of the electronic device.

16. The method of Claim 11, wherein exposing the electronic device to a plasma comprises controlling the exposure of the electronic device to the plasma to form a substantially perpendicular interface between the masked conductive material and the compound.

17. The method of Claim 11, wherein patterning a mask layer comprises patterning a photoresist layer outwardly from the conductive layer.

18. A method for forming a conductive pattern for an electronic device, comprising:

masking a portion of a conductive layer of the electronic device, the masked portion of the conductive layer defining the conductive pattern;

exposing the electronic device to a plasma **and at least one other gas selected from the group of inert gases and nitrogen**, the plasma converting an unmasked portion of the conductive layer into a compound **and the at least one other gas enhancing the conversion into the compound**; and

in a separate process from forming the compound, exposing the electronic device to a treatment process, the treatment process selectively removing the compound.

19. The method of Claim 18, wherein masking a portion of a conductive layer comprises depositing a photoresist layer outwardly from a portion of the conductive layer.

20. The method of Claim 19, further comprising removing the photoresist layer after removing the compound.

21. The method of Claim 19, further comprising removing the photoresist layer before removing the compound.

22. The method of Claim 18, wherein exposing the electronic device to a plasma comprises exposing the electronic device to a plasma, the plasma comprising a gas having an element selected from the halogen group of elements.

23. The method of Claim 22, wherein the plasma comprises a chlorine-containing gas.

24. The method of Claim 22, wherein the plasma comprises a bromine-containing gas.

25. The method of Claim 22, wherein the plasma comprises a fluorine-containing gas.

26. The method of Claim 22, wherein the plasma comprises an iodine-containing gas.

27. The method of Claim 18, wherein exposing the electronic device to a plasma comprises controlling the exposure of the electronic device to the plasma to form a substantially perpendicular interface between the masked conductive material and the compound.

28. The method of Claim 18, wherein the conductive layer comprises a copper material.

29. The method of Claim 28, wherein exposing the electronic device comprises exposing the electronic device to a plasma, the plasma comprising a chlorine-containing gas, the plasma converting the unmasked portion of the conductive layer to copper chloride.

30. The method of Claim 29, wherein exposing the electronic device to a treatment process comprises exposing the electronic device to a hydrogen chloride solution to remove the copper chloride.

31. **(New)** A method for forming a conductive pattern for a device, comprising:

patterning a mask layer outwardly from a conductive layer of the device, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing, by a plasma deposition reactor, the device to a plasma, the plasma converting the unmasked portions of the conductive layer into a compound; and

exposing the device to a treatment process, the treatment process selectively removing the compound.

32. **(New)** A method for forming a conductive pattern for a device, comprising:

patterning a mask layer outwardly from a conductive layer of the device, the patterning defining portions of the conductive layer where vias through the conductive layer are desired;

exposing the device to a low energy plasma, the plasma converting the unmasked portions of the conductive layer into a compound; and

exposing the device to a treatment process, the treatment process selectively removing the compound.